Reduction of Leakage Current and Power of Full Subtractor Using Mtcmos Technique

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Abstract: The invention of the first Integrated Circuit (IC) four decades ago, silicon technology down scaling continues to meet the increasing demands for higher functionality and better performance at a lower cost. Simulation result show reduction in both the leakage current and power using cadence tool in 45nm technology. Using 45nm technology for designing of full subtractor reduces in leakage current, power as well as area compared to conventional full subtractor. Reduction in leakage current is 15.63% and power is 95% compare to the conventional full subtractor.
Keywords: Intigatedcircuits(IC),conventionalsubtractor,powerlayout,leakagecurrent.

I. INTRODUCTION

Low-Power VLSI Design

Since the invention of the first Integrated Circuit (IC) four decades ago, silicon technology down scaling continues to meet the increasing demands for higher functionality and better performance at a lower cost. Power dissipation, though not entirely ignored, has been of little concern until recently. The advances in VLSI integration technology have made it possible to put a complete System on a Chip (SoC) which facilitates the development of portable systems. Portable battery- powered applications such as notebook computers, cellular phones, Personal Digital Assistants (PDAs), and military equipments profile power dissipation as a critical parameter in digital VLSI design.

With the increasing prominence of portable systems, it is important to prolong the battery life as much as possible, since it is the limited battery lifetime that typically imposes strict demands on the overall power consumption of such systems.

Although the battery industry has been making efforts to develop batteries with a higher energy capacity than that of conventional Nickel-Cadmium (NiCd) batteries, a revolutionary increase of the energy capacity does not seem imminent.

Power dissipation is also crucial for Deep Sub-Micron technologies. To further improve the performance of the circuits and to integrate more functions on a chip, the feature size has to continue to shrink. As a result, the power dissipation per unit area grows, increasing the chip temperature. Since the dissipated heat needs to be removed to maintain an acceptable chip temperature, large cooling devices and expensive packaging are required in portable devices and high-performance digital systems such as microprocessors. A recently announced Pentium IV 1 CPU, operating at a 3.4GHz frequency and 1.3V supply voltage, consumes 130W of power. Another important reason for low-power design is reliability. As technologies continue to scale, not only does the power density increase, but also the current density increases. Large current densities cause serious problems such as electro- migration and hot-carrier induced device degradation. In addition, the heat gradient across the chip causes thermal and mechanical stress leading to early breakdown. Therefore, the reliability can only be enhanced if power consumption is reduced Although power dissipation is important for modern VLSI design, performance (speed) and area are still the main requirements of a design. However, low-power design usually involves making tradeoffs such as timing versus power and area versus power. Increasing performance, while the power dissipation is kept constant, is also considered to be a low-power design problem.

Research Approach

The overall research approach for the sleep transistor sizing problem and the developed MTCMOS design environment are illustrated in Figure 1.
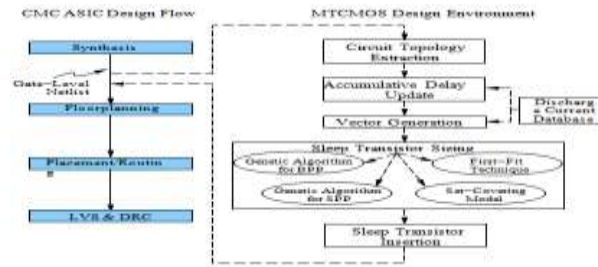
Figure 1: Overall approaches and developed MTCMOS environment

Within the MTCMOS design environment, several heuristic methods are de- veloped to handle the circuit extraction and vector generation. A discharge cur- rent database, based on the technology library, is also constructed. In addition, a CPLEX solver interfacing engine is built to identify the effectiveness of the Meta-heuristics for solving the BPP and the SPP, compared to the effectiveness of the CPLEX solver. Finally, a First-Fit (FF) technique and a Set-Covering (SC) model are proposed to effectively solve the sleep transistor sizing problem.

Full Subtractor

A full subtractor is a combinational circuit that performs a subtraction between two bits taking into account that a 1 may have been borrowed by a lower significant stage. This circuit has three inputs and two outputs. The three inputs A, B and C denote the minuend, subtrahend and previous borrow respectively.
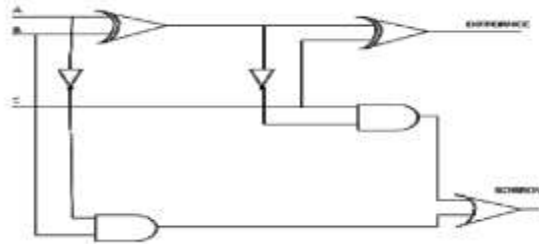
(a)

A	B	C	DIFF.	BORROW
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

TABLE I. TRUTH TABLE OF FULL SUBTRACTOR

(b)Figure 4: Schemetic and truth table of full-subtractor

The two outputs D and BORROW represent the difference and borrow, respectively. The logic circuit for full subtractor and the truth table for the full subtractor shown in Figure 4.The simplified Boolean functions for the outputs can be obtained directly from the truth table. The simplified logic equations are:

$$D = A'B'C + A'BC' + AB'C' + ABC$$

$$BORROW = C(A'B' + AB) + A'B$$

The low-power and high performance design requirements of modern VLSI technology can be achieved by using MTCMOS technology. This technique uses low, normal and high threshold voltage transistors in designing a CMOS circuit. Supply and threshold voltages are reduced with the scaling of CMOS technologies. Lowering of threshold voltages leads to an exponential increase in the sub threshold leakage current. The low-threshold voltage transistors which have high performance are used to reduce the propagation delay time in the critical path. The high-threshold voltage transistors which have less power consumption are used to reduce the power consumption in the shortest path. The multi threshold CMOS technology has two main parts. First, "active" and "sleep" operational modes are associated with MTCMOS technology, for efficient power management. Second, two different threshold voltages are used for N channel and P channel MOSFET in a single chip. These

apply on between the low threshold voltage (low-Vt) gates from the power supply and the ground line via cut-off high threshold voltage (high-Vt) sleep transistors is also known as "power gating".

Ultra Low Power / Ultra Low Voltage Circuit Design

The emerging self-sustaining applications such as intelligent sensor nodes stimulate the research on ultra low power circuit design. The primary issue associated with ultra low power circuit design is the choice of the power supply voltage. Since performance is typically not a critical issue, the power supply voltage of intelligent sensor nodes is typically scaled to minimize the energy consumption.

Due to the limited available energy with intelligent sensor nodes, the desirable (optimum) power supply voltage is the voltage level that minimizes the energy consumption per operation. The total energy consumption of an integrated circuit is primarily composed of dynamic switching energy consumption (E_{dyn}) and leakage energy consumption (E_{leak}). The dynamic switching energy consumption of a CMOS logic gate (assuming the output voltage swing of the logic gate is equal to V$_{DD}$) is

$$E_{dyn} = \alpha C V_{DD}^2 ,$$

where α is the switching activity factor. C is the total switching capacitance. The leakage energy that is consumed by a CMOS logic gate during one clock cycle is

$$E_{leak} = V_{DD} I_{off} T_{CLK} ,$$

where I_{off} is the sub-threshold leakage current that is produced by a CMOS logic gate. T_{CLK} is the clock period. The off-current of a transistor is

$$I_{off} = \mu C_{ox} \frac{W}{L} V_T^2 \exp\left(\frac{-|V_{th}|}{nV_T}\right)\left[1 - \exp\left(\frac{-|V_{DS}|}{V_T}\right)\right]$$

$$= \mu C_{ox} \frac{W}{L} V_T^2 \exp\left(\frac{-|V_{th0}| + \lambda_{DS}|V_{DS}| + \lambda_{BS}|V_{BS}|}{nV_T}\right)\left[1 - \exp\left(\frac{-|V_{DS}|}{V_T}\right)\right]$$

$$= I_0 \exp\left(\frac{\lambda_{DS}|V_{DD}|}{nV_T}\right)\left[1 - \exp\left(\frac{-|V_{DD}|}{V_T}\right)\right].$$

$$I_0 = \mu C_{ox} \frac{W}{L} V_T^2 \exp\left(\frac{-|V_{th0}| + \lambda_{BS}|V_{BS}|}{nV_T}\right).$$

μ, Cox, W, L, VT, and n are the carrier mobility, gate-oxide capacitance per unit area, transistor channel width, transistor channel length, thermal voltage, and sub-threshold swing coefficient, respectively. Vth is the transistor threshold voltage. $Vth0$ is the long channel transistor threshold voltage under zero body bias. The threshold voltage of transistor is modulated by the drain-to-source voltage (V_{DS}) through the drain induced barrier lowering coefficient (λ_{DS}) .Furthermore, the body-to-source voltage (V_{BS}) affects the threshold voltage of transistor through the body bias coefficient (λ_{BS}) .

The scaling of supply voltage results in approximately a quadratic reduction of dynamic energy consumption in both super-threshold and sub-threshold regions. The scaled V$_{DD}$ causes linear reduction of the voltage swing with the switching signals. In the super-threshold region, the on-current is reduced approximately linearly due to the velocity saturation phenomenon.The scaled V$_{DD}$ therefore results in approximately linear variation of T_{CLK}. Furthermore, the decrease of V$_{DD}$ causes exponential reduction of I_{off} in the super-threshold region. The leakage energy consumption is therefore reduced with lower V$_{DD}$ in the super- threshold region. The total energy consumption is suppressed with scaled V$_{DD}$ in the super- threshold region due to the reduction of both dynamic and leakage energy consumption. In the sub-threshold region, the switching-current (I_{switch}) of a transistor is

$$I_{switch} = \mu C_{ox} \frac{W}{L} V_T^2 \exp(\frac{|V_{GS}| - |V_{th}|}{nV_T}) \left[1 - \exp(\frac{-|V_{DS}|}{V_T}) \right]$$

$$= I_0 \exp(\frac{|V_{GS}|}{nV_T}) \exp(\frac{\lambda_{DS}|V_{DS}|}{nV_T}) \left[1 - \exp(\frac{-|V_{DS}|}{V_T}) \right]$$

$$= I_0 \exp(\frac{|V_{DD}|}{nV_T}) \exp(\frac{\lambda_{DS}|V_{DD}|}{nV_T}) \left[1 - \exp(\frac{-|V_{DD}|}{V_T}) \right].$$

Since the drain induced barrier lowering is less significant in the sub-threshold region, $\lambda_{DS} \ll 1$. Furthermore, by assuming that the power supply voltage is significantly higher than V_T (26mV at room temperature), the switching-current and off-current transistor in the sub-threshold region are simplified as

$$I_{switch} \approx I_0 \exp(\frac{|V_{DD}|}{nV_T}).$$

$$I_{off} \approx I_0.$$

The decrease of V_{DD} leads to exponential reduction of I_{switch}, thereby elongating T_{CLK} exponentially. The leakage energy consumption therefore tends to increase approximately exponentially in sub-threshold region. There is therefore an optimum power supply voltage (V_{DD_opt}) in the sub-threshold region which minimizes the total energy consumption per operation threshold region is the preferred region for ultra low power applications such as intelligent sensor nodes.A variety of challenges exist in sub-threshold circuit design. The ratio between the switching-current and off-current (I_{switch}/I_{off}) of a transistor is degraded remarkably in the sub-threshold region. By referring to equations 2.3 and 2.5, the I_{switch}/I_{off} is

$$I_{switch}/I_{off} = exp(V_{dd}/nV_t)$$

When the power supply voltage is scaled, the I_{switch}/I_{off} is reduced exponentially. Circuit topologies with a large number of transistors connecting to the same output node suffer from serious degradation in reliability. The total off-currents that are produced by the pull-down network could be comparable to the switching-current that is produced by P_1. The output voltage of the circuit cannot reach V_{DD}. Static DC current is therefore produced by the subsequent logic gates. If the degradation of the output voltage is significant, the entire circuit block can malfunction. Therefore, circuit topologies with high fan-in (popular in memory arrays and dynamic CMOS circuits) are prohibited in the sub-threshold circuit design.

The strength imbalance between PMOS and NMOS transistors is aggravated in the sub-threshold region, thereby degrading the noise margins of logic and memory circuits. The standard CMOS logic circuits behave as ratioed logic circuits. The strength imbalance between PMOS and NMOS transistors is increased with high fan-in circuit topologies. High fan-in logic gates (NAND and NOR logic gates with more than 3 inputs are therefore avoided in the standard cell libraries of sub-threshold logic circuits. Furthermore, the noise margins with memory elements, such as flip-flops and memory cells, are sensitive to the relative strengths of PMOS and NMOS transistors. The minimum voltage that is applicable to a sub-threshold circuit is typically determined by the noise margins of the memory elements. Transistor sizing is less effective in balancing the strength between PMOS and NMOS transistors in sub-threshold logic circuits.

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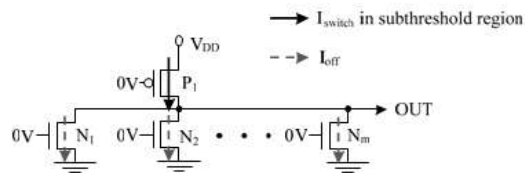
Figure 19: A CMOS gate with a large number of transistors that are connected to the output node.

Dsch And Microwind
The Nand Gate

The truth-table and logic symbol of the NAND gate with 2 inputs are shown below. In DSCH, select the NAND symbol in the palette; add two buttons and one lamp as shown above. Add interconnects if necessary to link the button and lamps to the cell pins. Verify the logic behavior of the cell.
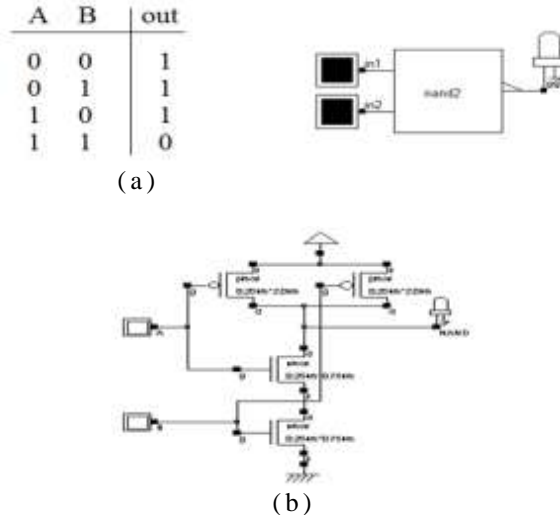

(a)

(b)

Fig 20: NAND gate(a)Truth-table and symbol.(b)schematic diagram of the CMOS NAND gate design.

MOS layout

We use MICROWIND2 to draw the MOS layout and simulate its behavior. Go to the directory in which the software has been copied (By default MICROWIND2). Double-click on the MicroWind2 icon.
The MICROWIND2 display window includes four main windows: the main menu, the layout display window, the icon menu and the layer palette. The layout window features a grid, scaled in lambda (□) units. The lambda unit is fixed to half of the minimum available lithography of the technology. The default technology is a CMOS 6-metal layers 0.25µm technology, consequently lambda is 0.125 µm.

Fig. 21 a) T h e MICROWIND2 window as it appears at the initialization stage.

The palette is located in the lower right corner of the screen. A red color indicates the current layer. Initially the selected layer in the palette is polysilicon. By using the following procedure, you can create a manual design of the n-channel MOS.

Static Mos Characteristics

Click on the MOS characteristics icon. The screen shown in Figure 21(b) **appears. It represents the Id/Vd static characteristics of the *nMOS device***
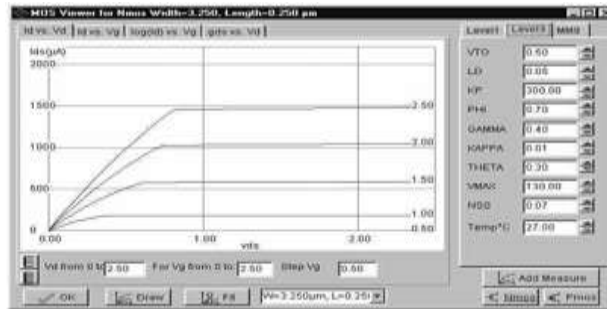

Fig. 21(b): N-Channel MOS characteristics.

The MOS size (width and length of the channel situated at the intersection of the polysilicon gate and the diffusion) has a strong influence on the value of the current. The MOS width is 3.25µm and the length is 0.25µm. A high gate voltage (Vg =2.5V) corresponds to the highest Id/Vd curve. For Vg=0, no current flows. A maximum current around 1.5mA is obtained for Vg=2.5V, Vd=2.5V, with Vs=0.0. The MOS parameters correspond to SPICE Level 3. A tutorial on MOS model parameters is proposed later in this chapter. . The MOS width is 3.25µm and the length is 0.25µm. A high gate voltage (Vg =2.5V) corresponds to the highest Id/Vd curve. For Vg=0, no current flows.

Dynamic MOS behavior

This paragraph concerns the dynamic simulation of the MOS to exhibit its switching properties. The most convenient way to operate the MOS is to apply a clock to the gate, another to the source and to observe the drain. The summary of available properties that can be added to the layout is reported below.
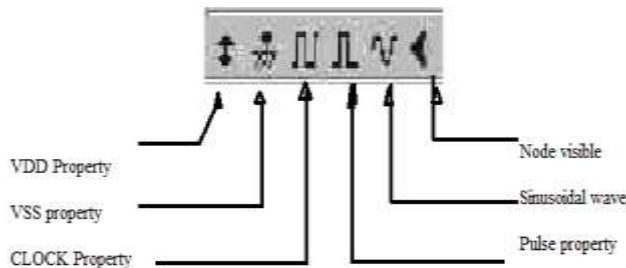
Apply a clock to the gate. Click on the Clock icon and then, click on the polysilicon gate. The clock menu appears again. Change the name into « Vgate» and click on OK to apply a clock with 2.1ns period (1ns at 0, 50ps rise, 1ns at 1, 50ps fall).

Fig. 21(c): The clock menu.

Apply a clock to the drain. Click on the Clock icon, click on the left diffusion. The Clock menu appears. Change the name into « Vdrain » and click on OK. A default clock with 4.2ns period is generated. The Clock property is sent to the node and appears at the right hand side of the desired location with the name « Vdrain ». Watch the output: Click on the Visible icon and then, click on the right diffusion. Click OK. The Visible property is then sent to the node. The associated text « s1 » is in italic, meaning that the waveform of this node will appear at the next simulation. Always save BEFORE any simulation. The analog simulation algorithm may cause run-time errors leading to a loss of layout information. A default clock with 4.2ns period is generated. The Clock property is sent to the node and appears at the right hand side of the desired location with the name « Vdrain ».Click on **File** -> **Save as** . A new window appears, into which you enter the design name. Type, for example, **myMos**. Then click on 'Save'. The design is saved under that filename.

Analog Simulation

When the gate is at zero, no channel exists so the node s1 is disconnected from the drain. When the gate is on, the source copies the drain. It can be observed that the nMOS device drives well at zero but poorly at the high voltage. The highest value of s1 is around 2.0V, that is VDD minus the threshold voltage. This means that the n-channel MOS device do not drives well logic signal 1. Click on **More** in order to perform more simulations. Click on **Close** to return to the editor.

The safest way to create a MOS device is to use the MOS generator. In the palette, click the MOS generator icon. A window appears as reported below. The programmable parameters are the MOS width, length, the number of gates in parallel and the type of device (n-channel or p-channel). By default metal interconnects and contacts are added to the drain and source of the MOS. You may add a supplementary metal2 interconnect on the top of metal 1 for drain and source.
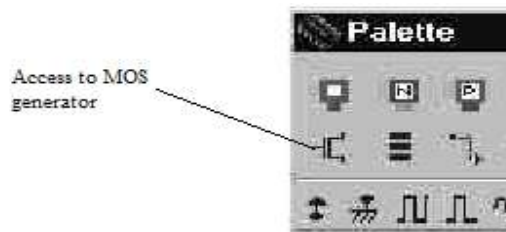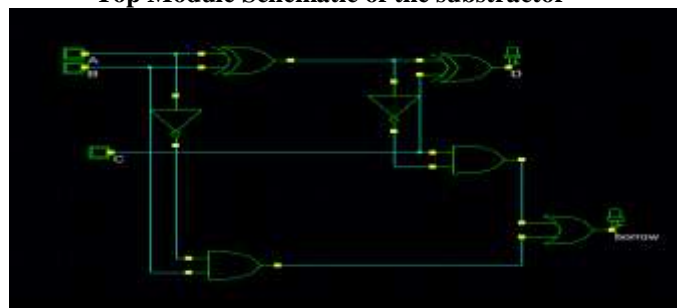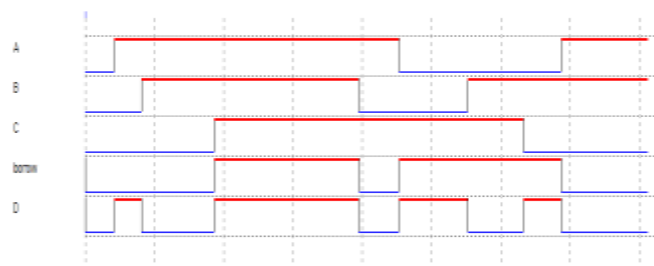

Fig. 21(e): Analog simulation of the MOS device.

RESULTS
Top Module Schematic of the substractor

(a)


(b)

TABLE I.   TRUTH TABLE OF FULL SUBTRACTOR

| A	B	C	DIFF.	BORROW
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

(c)

Figure 22: Subtractor.(a) Schematic, (b) Simulation and (c) Truth table

The above schematic represent the gate design of the proposed substractor .the schmetaic is drawn using dsch software . The above simulation shows the A,B,C input of the subtractor .d is the difference calculated and the borrow is the carry left .The difference is the substraction between a and b in the above truth table .the carry left is the borrow .

Substactor using MT cmos technique
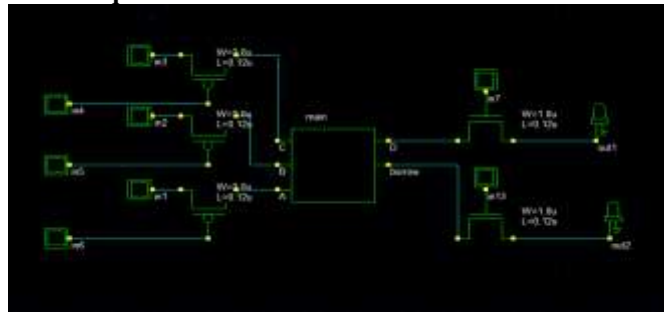
(a
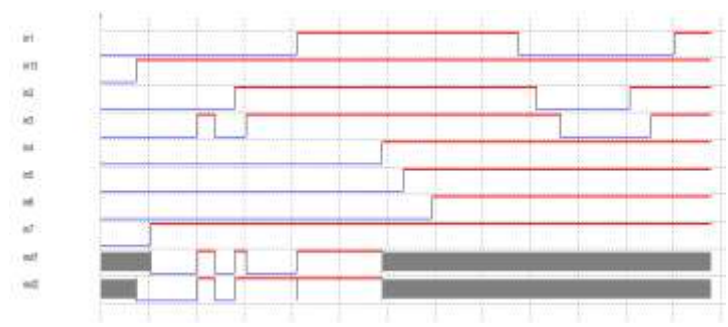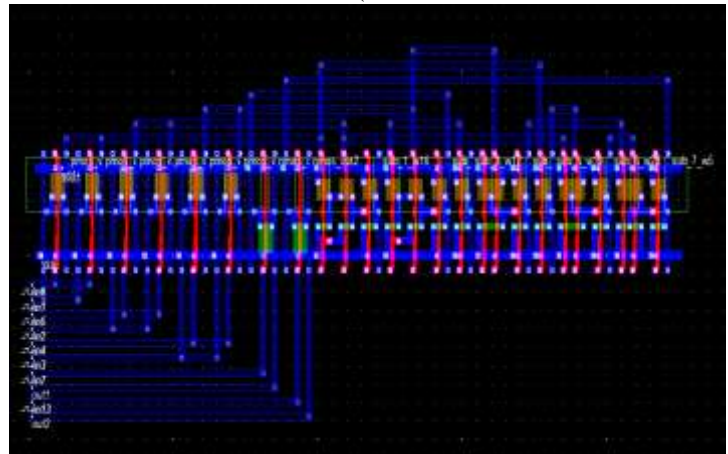
(b)
**fig 23:** MTCMOS Subtrctor. (a) Schematic and (b) Simulation

A full subtractor subtracts 3input bits and gives the output in the form of difference and borrows. We design the transistor level full subtractor using cadence virtuoso tool in 45 nm technology and simulate it giving the inputs and get output. By applying the MTCMOS technique in 45nm technology reduction in current and power

Power report

Figure 25: Power consumed in the microwind software

Logical output
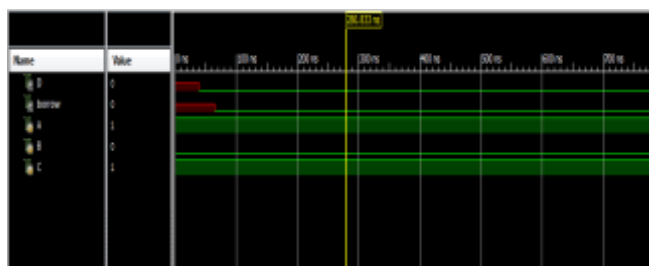
II. CONCLUSION

Simulation result show reduction in both the leakage current and power using cadence tool in 45nm technology. Using 45nm technology for designing of full subtractor reduces in leakage current, power as well as area compared to conventional full subtractor. Reduction in leakage current is 15.63% and power is 95% compare to the conventional full subtractor.

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